description

1. GENERAL

This section presents the purpose, specifications, general description, and principles of operation of the 514A-3 Radio Set Control (CPN 792-6121-001, -101, -201) and 514A-4 Radio Set Control (CPN 792-6122-XXX).

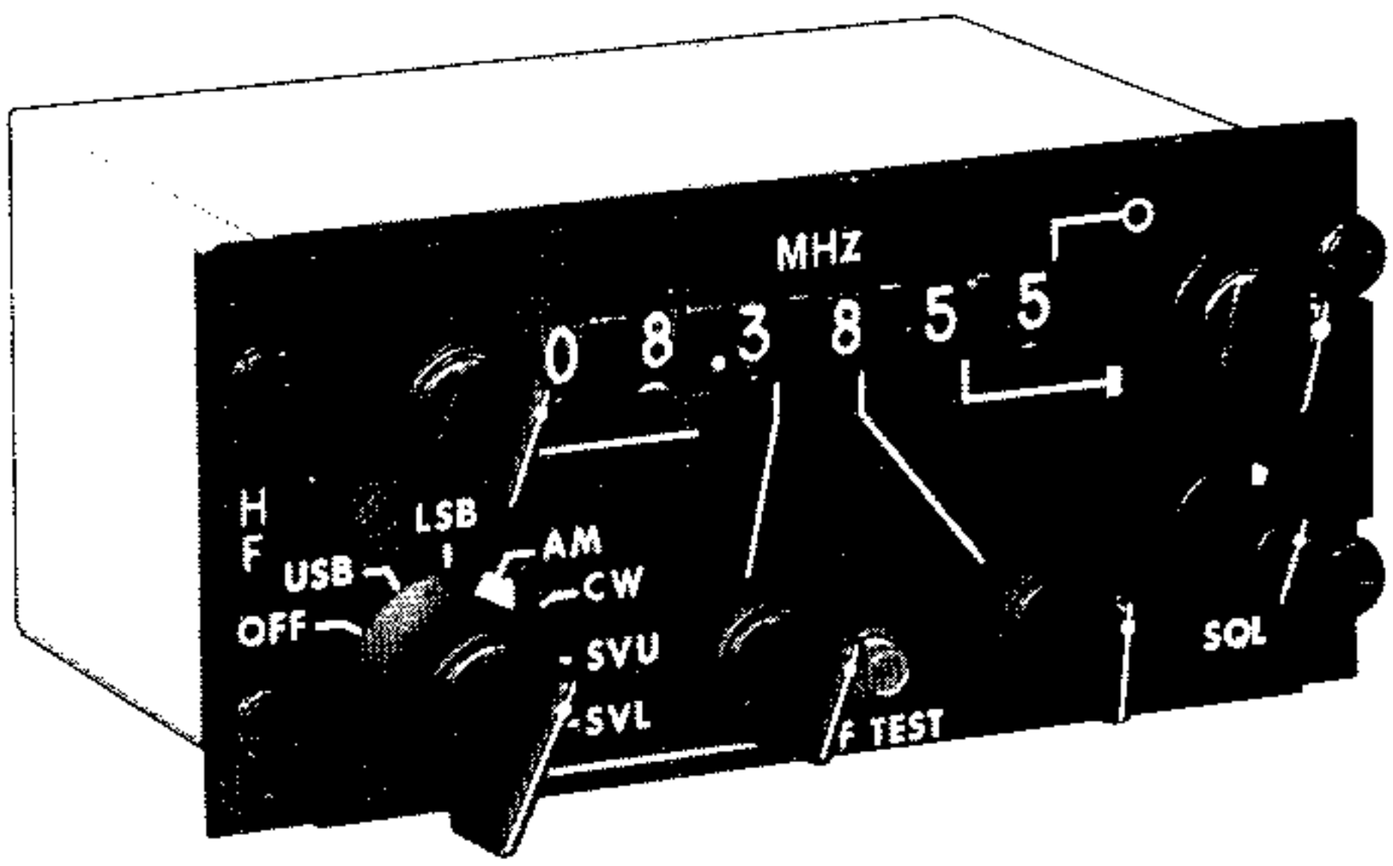
2. PURPOSE OF EQUIPMENT

The 514A-3/4 Radio Set Control (figure 1) permits manual control of an hf communication system that uses serial-digital techniques. The equipment supplied is listed in table 1.

3. EQUIPMENT SPECIFICATIONS

3.1 Electrical Specifications

Frequency range	2 to 29.9999 MHz.
Frequency channels	280 000 in 100-Hz increments.
Operational modes	USB, LSB, AM, CW, narrow band secure voice (SVU OR SVL), and RF TEST on all units except as listed in table 2 difference data.
Front panel lighting	28- or 5-volt edge lighting per MIL-P-7788C type V, class 1-W. (See table 2.)
Power requirements	28 V at 150 mA or 5 V at 600 mA nominal, for panel lighting; 28 V dc for RF TEST lamp (from rcvr/exctr unit): +15 volts dc continuous (from rcvr/exctr unit).



TP2-4506-017

514A-3/4 Radio Set Control
Figure 1

3.2 Environmental Specifications

Altitude .....0 to 12 192 m (0 to 40 000 ft).

Temperature .....-55 to +71 °C (-65 to +160 °F).

Humidity .....Up to 95% relative at 50 °C (+122 °F).

Vibration .....±2 g at 55 to 500 Hz.

Crash safety .....30 g in each of three planes.

Table 1. Equipment Supplied.

SUBASSEMBLY/ CIRCUIT CARD		RADIO SET CONTROL														
		514A-3			514A-4											
TITLE	COLLINS PART NUMBER	792-6121-( )			792-6122-( )											
		-001	-101	-201	-001 -101 -201	-002 -102 -202	-003 -103 -203	-004 -104 -204	-005 -105 -205	-007 -107 -207	-009 -109 -209	-010 -110 -210	-011 -111 -211	-012 -112 -212	-013 -113 -213	-014 -114 -214
Front panel assembly	790-1829-001 790-1829-002 790-1829-003 790-1829-004 790-1829-005 790-1829-006 790-1829-007 790-1829-008 790-1829-009 790-1829-010 790-1829-011 790-1829-012	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X
+15-V DC to +5-V DC converter A1	609-0681-001 or 790-2505-001	X	X		3	3	3	3	3	3	3	3	3	3	3	3
Modulo-two transmit card A2	793-9264-001 642-3591-001 642-3591-002	X	X	X	4 1 2	4 1 2	4 1 2	4 1 2	4 1 2	4 1 2	4 1 2	4 1 2	4 1 2	4 1 2	4 1 2	4 1 2

Note

1. Used by -1XX series status only
2. Used by -2XX series status only
3. Not used by -2XX series status only
4. Used by -0XX series status only

4. PHYSICAL DESCRIPTION

The 514A-3/4 Radio Set Control chassis is made of aluminum and is designed for 4-point console mounting. The control is mounted using four Dzus fasteners located on the front panel (figure 1). Electrical connections to the control are made through a connector located on the rear of the unit (see outline and mounting dimensions diagram in the diagrams section of this manual). One plug-in printed circuit board contains logic circuits to convert the parallel wire control information from rotary switches into serial-digital output. A shielded submodule contains a dc-to-dc converter to provide +5 V dc for the logic circuits. (This dc-to-dc converter is not used in the -2XX series control.) The selected operating frequency is displayed by a mechanical digital indicator on the front panel. For controls and indicator functions and descriptions refer to the operation section of this instruction book.

5. PRINCIPLES OF OPERATION

5.1 General

The 514A-3/4 Radio Set Control provides a manual input for frequency selection, mode (function) selection, and squelch control of an associated hf communication system. Control information is transferred to the hf system by a serial-digital control word transmitted through a shielded, twisted-pair control bus.

The 514A-3/4 provides a selection of 280 000 communications channels covering the frequency range from 2.0000 to 29.9999 MHz in 100-Hz increments. Frequency selection is made by positioning five frequency selector switches on the front panel. A mode selector switch on the front panel provides a selection of upper sideband (USB), lower sideband (LSB), amplitude modulation (AM), continuous wave (CW), narrow band secure voice upper (SVU), narrow band secure voice lower (SVL), or RF TEST. A squelch (SQL) control, also on the front panel, provides a selection of eight squelch threshold level settings for the audio circuits in the associated hf system. Single-line inputs through the rear connector are available for ptt keying, pilot carrier enable, and external rechannel lines controlled by external remote switches. The control information selected by positioning the five switches on the front panel is a parallel binary coded decimal (bcd) signal. The logic circuits convert the parallel control information into a 32-bit control word that is transmitted serially through a single-pair 2400-Hz bus.

Front panel lighting of the 514A-3/4 is of the edge lighting type at 28 or 5 volts dc or ac, with color as indicated in table 2.

5.2 Functional Theory

5.2.1 General

The desired control instructions are inserted into the 514A-3/4 Radio Set Control by positioning the control switches located on the front panel. A push-to-talk (key) switch, for control of voice communications, is located on the operator's microphone. The control switches provide binary coded decimal (bcd) information, in parallel form, to the modulo-two transmit card A2. The following paragraphs will discuss modulo-two transmit card A2 793-9264-001 and 642-3591-001, -002.

5.2.2 A2 793-9264-001 (Refer to figure 2)

Modulo-two transmit card A2 accepts the parallel binary signals from the control switches, develops a control data word from these inputs, and transmits the control word in bit serial mode to the receiver-exciter.

All timing signals used by the 514A-3/4 are derived from a single source, an astable multivibrator located on A2 and operating at 4800 Hz ±5 percent. The 4800-Hz output of the multivibrator is applied to the timing generator circuit that provides timing (clock) signals throughout the 514A-3/4.

Control information, in binary parallel form, is applied from the control switches to a 32-bit parallel-to-serial converter circuit. The serial data output of the converter is applied through a data gate circuit to an exclusive OR circuit where it is combined (modulo-two added) with the 2400-Hz bit clock signal. The output of the exclusive OR circuit forms the serial data control signal that is applied to a line driver stage to provide a dc balanced, differential signal for the serial-digital output. The data control word contains all of the information to be transmitted from the 514A-3/4 to the receiver-exciter unit.

The control word consists of 32 discrete bits in the format specified below (shown in figure 3) with bit 1 transmitted first and bit 32 transmitted last.

BIT	FUNCTION	DESCRIPTION
1	Key signal	Transmit mode - logic 1 Receive mode - logic 0
2	Pilot carrier enable	Enable - logic 1 Disable - logic 0
3 through 5	Squelch level	Bit 3 is the least and bit 5 is the most significant bit. A data value (digit weight) of 0 corresponds to the maximum squelch threshold level and a data value of 6 corresponds to the minimum squelch threshold level. A data value of 7 disables the squelch circuits.
6 through 8	Mode select	Bit 6 is the least and bit 8 is the most significant bit.
9 through 30	Frequency select	Conventional bcd 4-bit coding is used, least significant digit first. The frequency digits are oriented with the least significant digit first (ie, 100 Hz is coded into bits 9 through 12, 1 kHz is coded into bits 13 through 16, etc). The 10-MHz digit is shortened to two bits (bits 29 and 30) since it may assume only the values of 0, 1, or 2.
31	Tune start	Indicates that control has been turned on or that a frequency setting has been changed. The change condition has a binary weight of logic 1 and is maintained for four to eight consecutive word times after disappearance of the tune start signal. The logic then reverts to the no-change condition which has a binary weight of logic 0.
32	Word sync	Used to frame (ie, identify a known position) the data control word. The binary weight (logic level) of the word sync bit alternates for consecutive word transmissions.

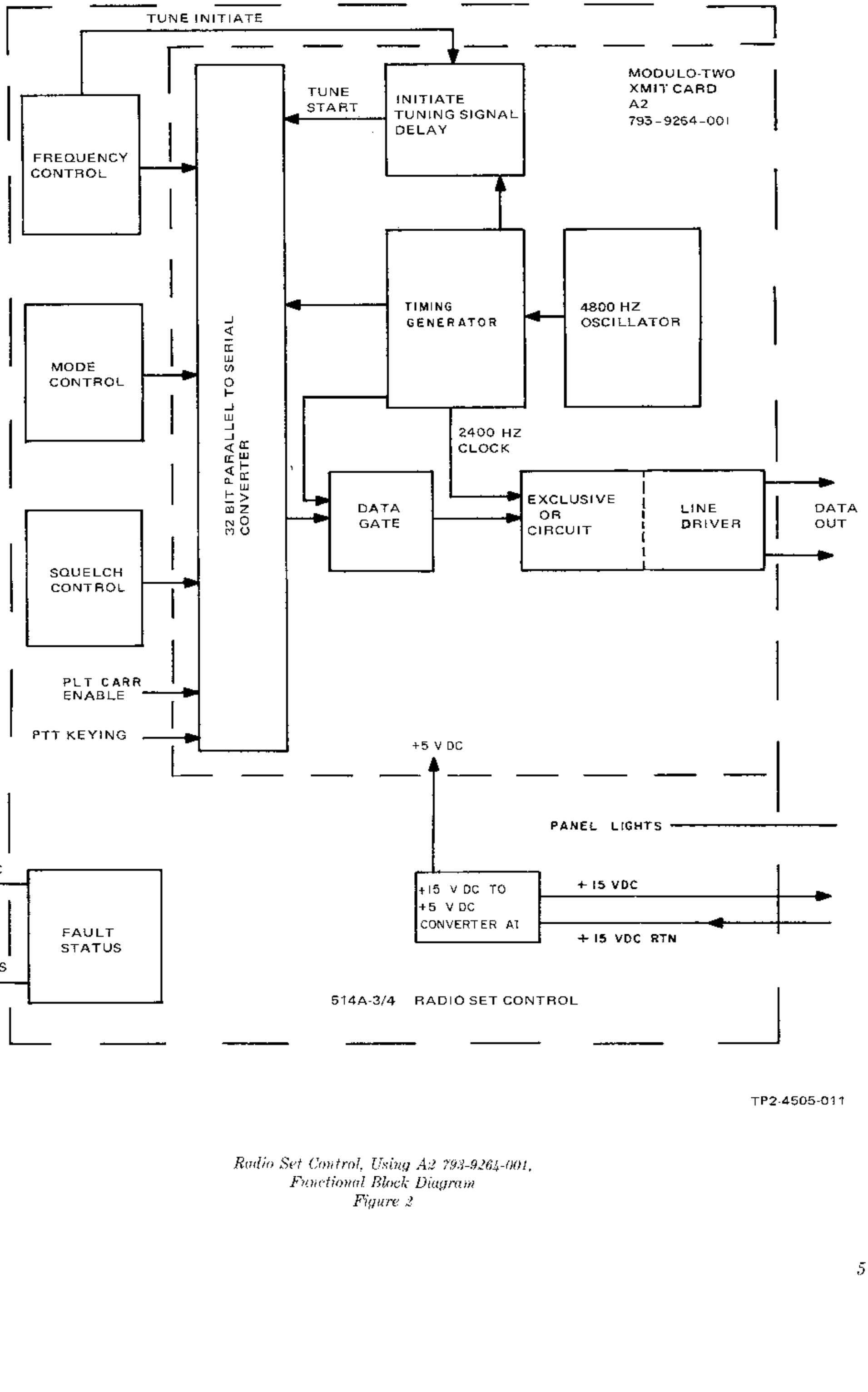
The serial control data signal is the only output from the 514A-3/4. The output is a dc-balanced differential signal that operates into a shielded, twisted pair of #22 AWG wires not longer than 152 m (500 ft) and that is terminated by an impedance of 82 ohms ±10 percent (resistive). The characteristics specified for the signal waveshape are defined in figure 4.

The operational status of the system can be monitored with the RF TEST lamp (fault status) located on the front panel. With the 514A-3/4 in the RF TEST mode and the system keyed, the fault monitoring circuits in the receiver-exciter are enabled. If a fault is detected, the RF TEST lamp will be switched on by the receiver-exciter circuits. A steady glow or a flashing indication may be used to indicate a fault in one of the units in the hf system.

5.2.3 A2 642-3591-001, -002 (Refer to figure 5)

Modulo-two transmit card A2 642-3591-001, -002 accepts the parallel binary signals from the control switches, develops a control data word from these inputs, and transmits the control word in bit serial mode to the receiver-exciter.

The timing signals used by the 514A-3/4 are derived from a single source, a 4800-Hz oscillator. The 4800-Hz output of the oscillator is applied to divider U2 and to the reset input of U4A. Divider U2 changes the 4800-Hz input frequency to the 2400-Hz clock frequency and applies this signal to U9B. The output of U9B (2400-Hz clock) is applied to parallel-to-serial converter U5 through U8 and also to exclusive OR circuit U1C.



TP2-4505-011

Radio Set Control, Using A2 793-9264-001,
Functional Block Diagram
Figure 2

Control information, in binary parallel form, is applied from the control switches to 32-bit parallel-to-serial converter circuit U5 through U8.

The serially clocked data output of the converter is applied to an exclusive OR circuit where it is combined (modulo-two added) with the 2400-Hz clock signal. The output of the exclusive OR circuit forms the serial data control signal that is applied to a line driver stage (U9A) to provide a dc balanced, differential signal for the serial-digital output. The data control word contains all of the information to be transmitted from the 514A-3/4 to the receiver-exciter unit.

The control word consists of 32 discrete bits in the format shown in figure 3, with bit 1 transmitted first and bit 32 transmitted last.

The +15-V DC to +5-V DC converter A1 is used with A2 642-3591-001, but not used with A2 642-3591-002.

5.3 Detailed Theory

5.3.1 General

Discussion of detailed theory will be accomplished by discussing the front panel controls, module-two transmit card A2, +15-V DC to +5-V DC converter A1, and power on tune initiate circuit.

5.3.2 Front Panel Control

The control switches located on the front panel of the 514A-3/4 provide three functional input signals to modulo-two transmit card A2. These control signals are: operating mode, squelch level, and frequency selection. A ptt keying signal or a pilot carrier enable signal may be provided by external control switches presenting high (greater than 100 kilohms) or low (less than 100 ohms) resistances to ground on individual lines to the 514A-3/4 rear connector. Refer to corresponding figures in the diagrams section for connector pin information.

The frequency, mode, and squelch level signals are switched connections to ground developed by the control switches on the front panel. The status of each switch contact is tested by a sensing circuit that has an open circuit voltage of +5.0 ±0.5 V dc (referenced to ground) and a source impedance of 3900 ohms ±10 percent.

The frequency signal consists of 23 input lines representing five full binary coded decimal digits, one abbreviated binary coded decimal digit, and an initiate (tune start) signal. The initiate signal is a momentary switch closure to ground which occurs whenever any frequency selection switch is moved from a detented position.

The mode signal consists of three input lines that code eight possible operating mode selections (figure 13 or 14 in the diagrams section). The mode selection switch has shorting type switch contacts.

The squelch signal consists of three input lines which code eight possible squelch level settings (figure 13 or 14 in the diagrams section).

The ptt keying signal and the pilot carrier enable signal are each a single line input signal developed externally; these may be either a switch contact closure or a saturated transistor-type switch closure to ground. Impedance for the closed switch condition shall not exceed 100 ohms, and for an open switch condition shall be not less than 100 kilohms. The keying signal and pilot carrier enable signal are sensed by circuits having an open circuit voltage of +5.0, +0.335, and -0.5 V dc (referenced to ground) and a source impedance of 3900 ohms ±10 percent. Overvoltage protection is provided by 5.1-volt zeners (VR1 and VR2) on modulo-two transmit card A2 (on 793-4264-001 only).

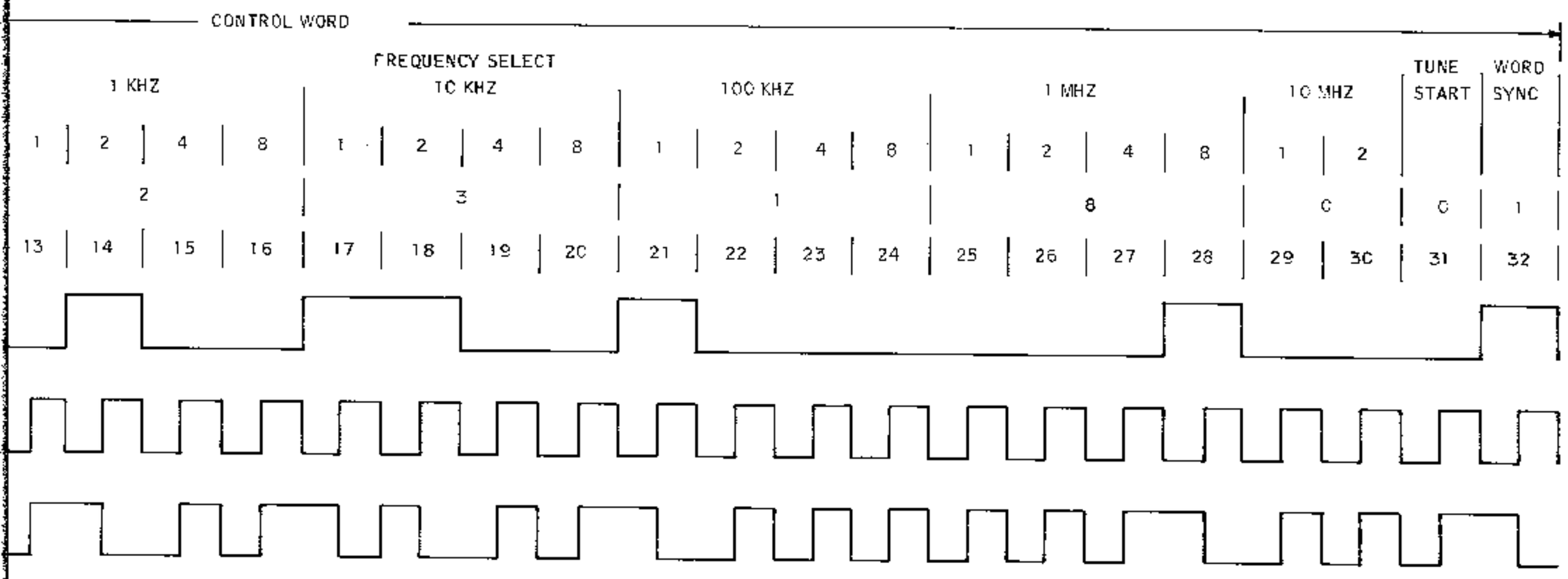
5.3.3 Modulo-Two Transmit Card A2

5.3.3.1 General

Modulo-two transmit card A2 interfaces the 514A-3/4 controls with the modulo-two receive assembly in a remotely located receiver-exciter. Card A2 accepts all of its input signals in parallel, develops the control data word from these inputs, and transmits the control word in serial bit mode to the receiver-exciter. In the following paragraphs, two versions of the A2 will be discussed: 793-9264-001 and 642-3591-001, -002.

5.3.3.2 A2 793-9261-001

All internal timing signals required by A2 793-9264-001 are derived from the 4800-Hz astable multivibrator Q1 and Q2. The output of the multivibrator is routed through logic inverters U5C and U5D and applied to the timing generator circuit (U6 and U1). The timing generator circuit is basically two divide-by-16 binary counters connected in series. By divider action, the timing generator develops the 2400-Hz clock signal plus seven difference timing signals. Each timing signal has a specific binary weight, WT1,

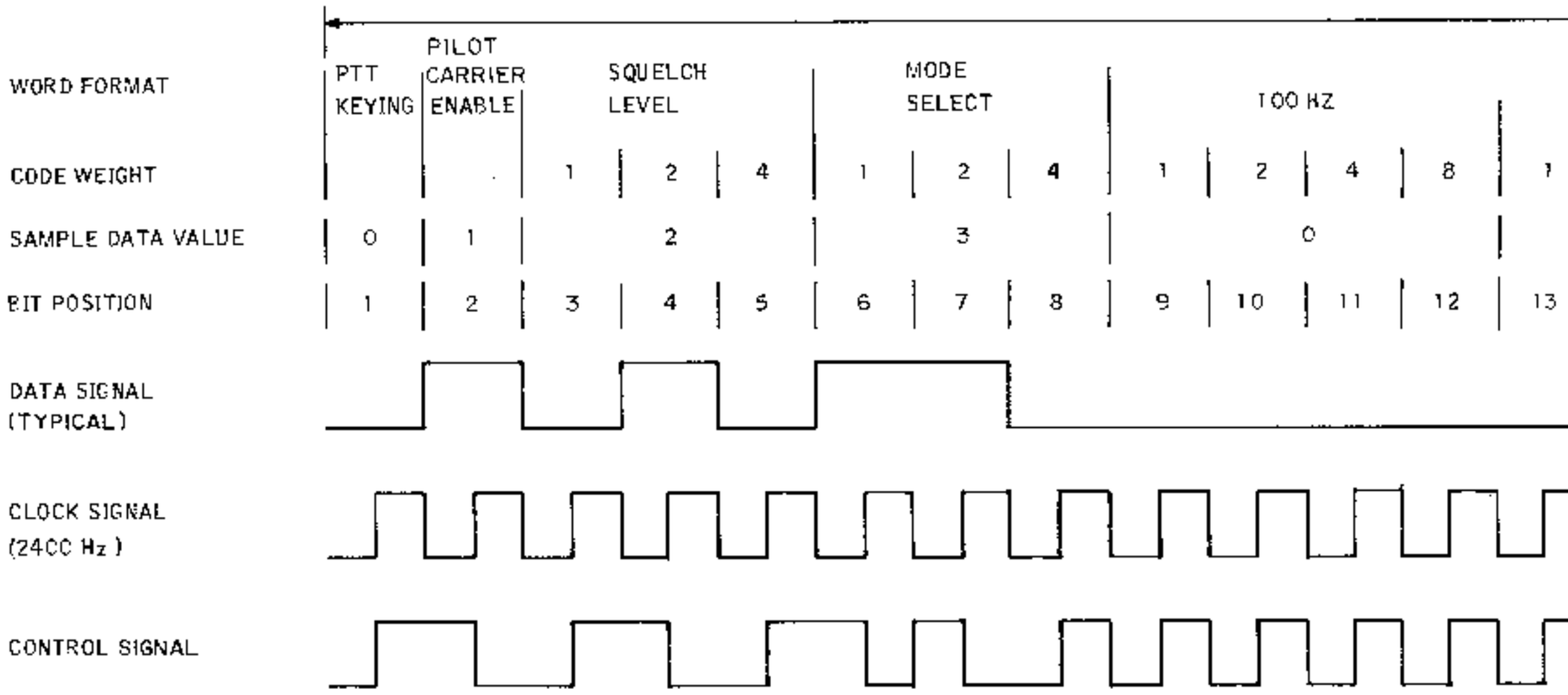


CHARACTERISTIC	DATA CODING	DATA VALUE
FREQUENCY SELECT		
100 Hz DIGIT (BITS 9-12)		
0 Hz	0000	0
100	0001	1
200	0010	2
300	0011	3
400	0100	4
500	0101	5
600	0110	6
700	0111	7
800	1000	8
900	1001	9
1 kHz DIGIT (BITS 13-16)		
0 kHz	0000	0
1	0001	1
2	0010	2
3	0011	3
4	0100	4
5	0101	5
6	0110	6
7	0111	7
8	1000	8
9	1001	9
10 kHz DIGIT (BITS 17-20)		
00 kHz	0000	0
10	0001	1
20	0010	2
30	0011	3
40	0100	4
50	0101	5
60	0110	6
70	0111	7
80	1000	8
90	1001	9

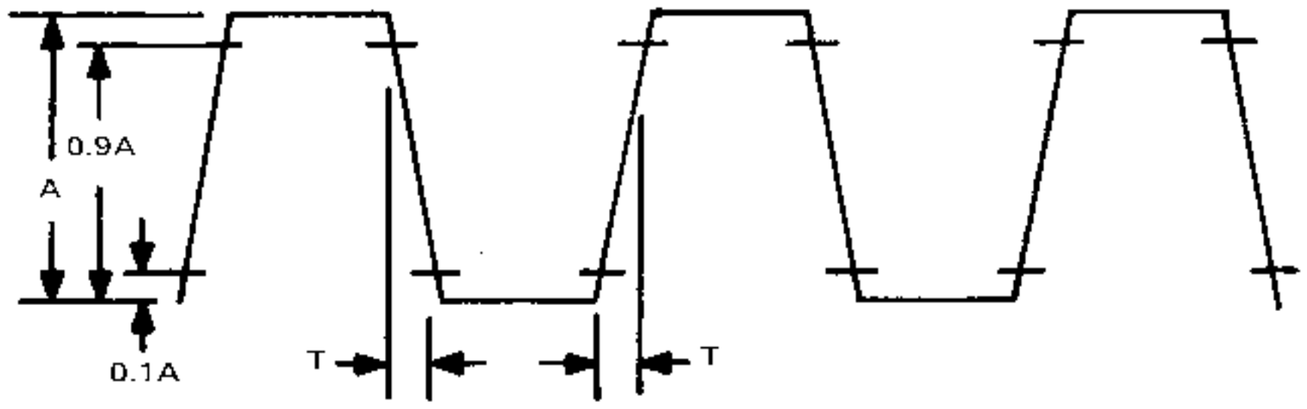
CHARACTERISTIC	DATA CODING	DATA VALUE
FREQUENCY SELECT		
100 kHz DIGIT (BITS 21-24)		
000 kHz	0000	0
100	0001	1
200	0010	2
300	0011	3
400	0100	4
500	0101	5
600	0110	6
700	0111	7
800	1000	8
900	1001	9
1 MHz DIGIT (BITS 25-28)		
0 MHz	0000	0
1	0001	1
2	0010	2
3	0011	3
4	0100	4
5	0101	5
6	0110	6
7	0111	7
8	1000	8
9	1001	9
10 MHz DIGIT (BITS 29, 30)		
00	0000	0
01	0001	1
10	0010	2
TUNE START (BIT 31)		
LOGIC 1		1 FOR AT LEAST 4 WORDS AFTER A NEW FREQUENCY IS SELECTED
LOGIC 0		0 ALL OTHER TIMES
WORD SYNC		
BIT 32		1 OR 0 LOGIC LEVEL ALTERNATES EACH SUCCESSIVE WORD

TP2-3904-014

Modulo-Two Control Word Format
Figure 3



CHARACTERISTIC	DATA CODING	DATA VALUE
PTT KEYING		
TRANSMIT	1	1
RECEIVER	0	0
PILOT CARRIER ENABLE		
ENABLE	1	1
DISABLE	0	0
SQUELCH LEVEL		
HIGHEST THRESHOLD	000	0
	001	1
	010	2
	011	3
	100	4
	101	5
LOWEST THRESHOLD	110	6
DISABLE	111	7
MODE SELECT		
OFF	000	0
USB	001	1
LSB	010	2
AME	011	3
CW	100	4
SVU	101	5
SVL	110	6
TEST	111	7



A = 3,6 ± 1.5 VOLTS
T = RISE/FALL TIME
SIGNAL DURATION DEPENDS UPON THE DATA.

TP2-4656-011

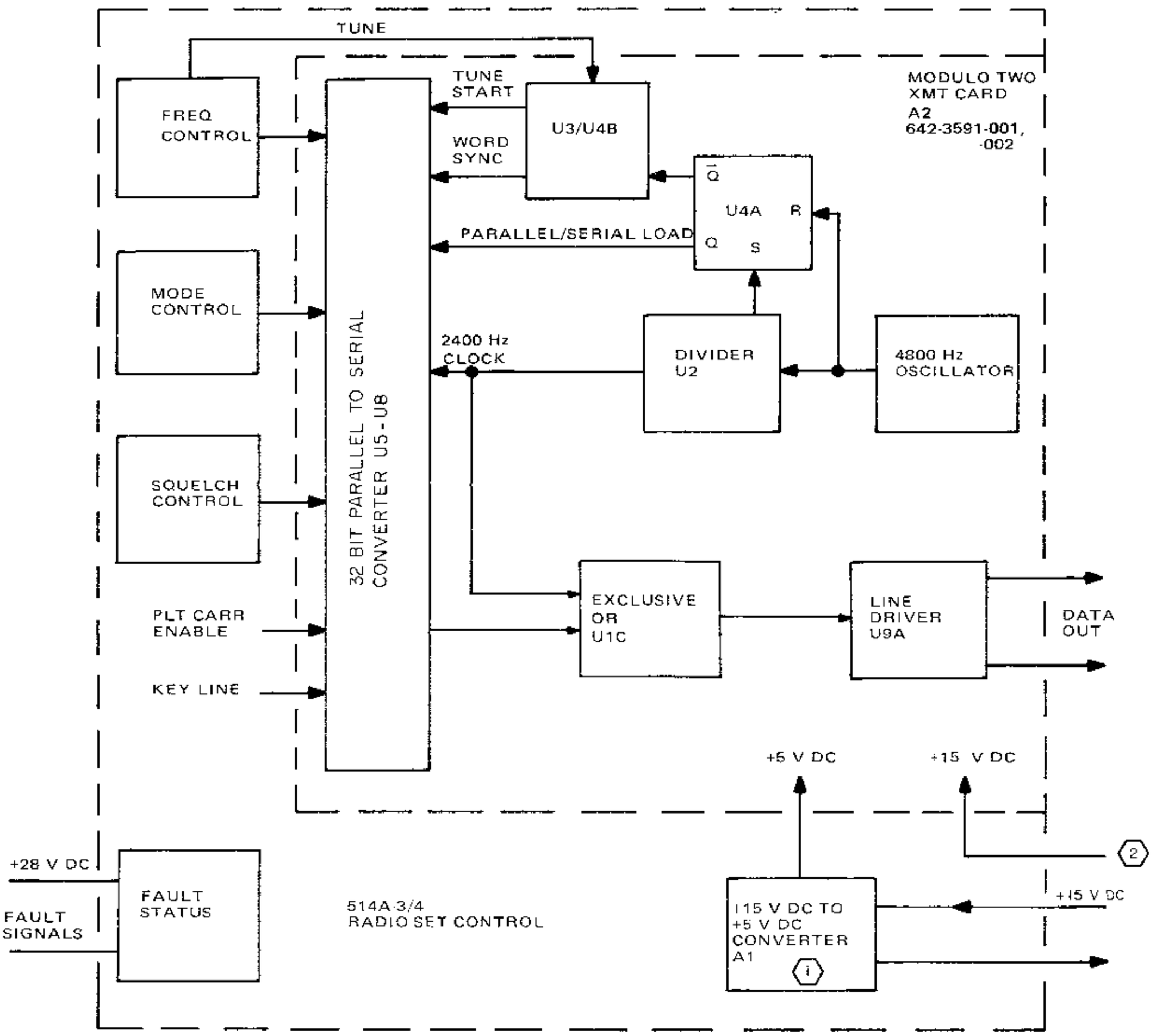
Output Signal Waveform
Figure 4

WT2, WT4, WT8, WT16, WT32, and WT64 (figure 6). Timing signals WT1, WT2, and WT4 from counter U6 are applied to pins 11, 12, and 13 of the four 8-bit multiplexers, U2, U7, U4, and U9. The WT4 signal is also applied to the clock input of the second counter U1. An enable signal, timing signal WT8, is applied directly to pin 10 of multiplexers U2 and U7; simultaneously, timing signal WT8 is inverted through logic gate U5A and applied to pin 10 of multiplexers U4 and U9.

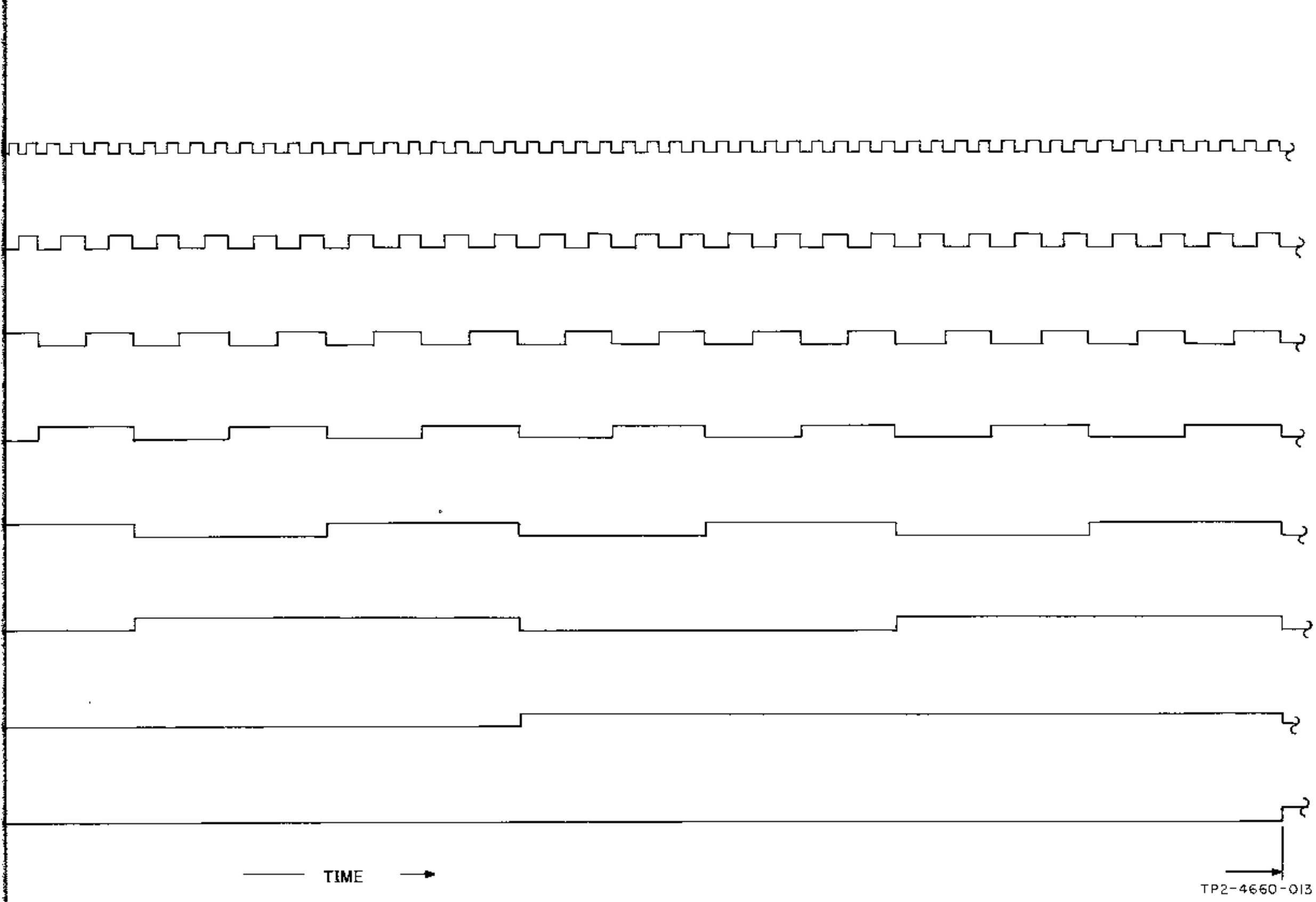
Only two multiplexers are enabled at any given time (U2 and U7 or U4 and U9). Timing signal WT16 from U1 in both direct and inverted states is applied to data gate circuit U11, so that either logic gates A and B or C and D will be enabled at any given time. Timing signal WT32 is applied to pin 9 of multiplexer U9, and timing signal WT64 is used as the clock signal for the initiate tuning signal delay circuit (U3).

Selected control information (key enable, squelch level, operating mode, and frequency selection) is applied in inverted form to the appropriate multiplexer. The output signal from the multiplexers (pin 15), along with the WT16 timing signal, is applied to data gate circuit U11. Data gate U11 allows only the appropriate control data (determined by the timing signals) to be routed to the exclusive OR circuit where it is modulo-two added with the 2400-Hz clock signal from the timing generator circuit. For example, operating mode control information is included in bits 6, 7, and 8. Assume a time period in which multiplexers U2 and U7 are enabled, U4 and U9 are disabled, logic gates C and D of U11 are enabled, and logic gates A and B of U11 are disabled. Only the output (mode selection) of U2 is passed through data gate U11 to the exclusive OR circuit (U5B, U5E, U8A, and U8B).

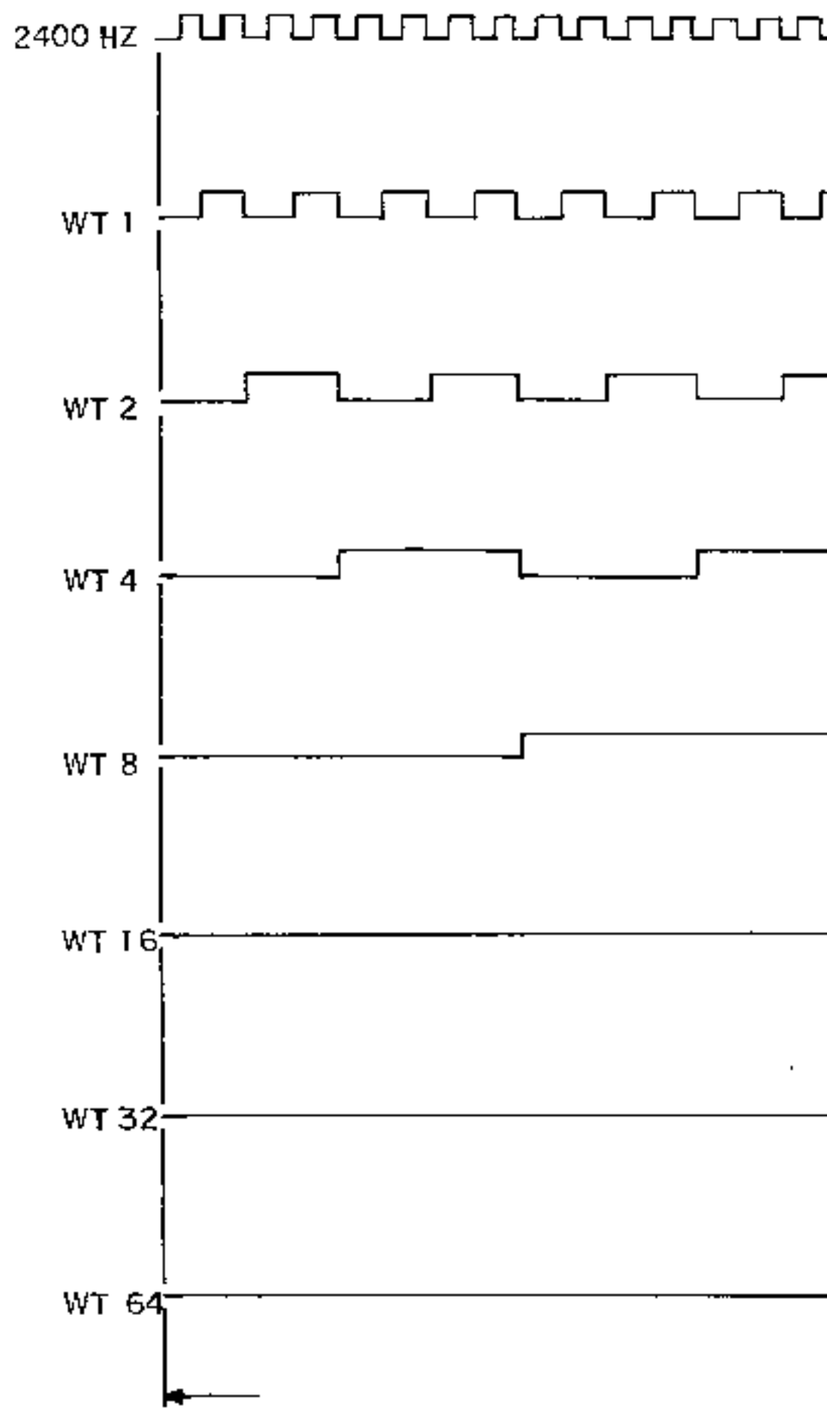
The serial control data and the 2400-Hz clock signal are simultaneously applied in both direct and inverted state to logic gates U8A and U8B. When the serial control data and 2400-Hz clock signal are in phase (both logic 1 or logic 0), the outputs of U8A and U8B will be inverted from each other (see figure 13 in the diagrams section) applying a logic 1 and a logic 0 to input pins 1 and 2 of line driver U10A. When the serial control data and 2400-Hz clock signal are out of phase, the outputs of U8A and U8B will be a logic 1, applying a logic 1 to input pins 1 and 2 of line driver U10A. When the inputs of U10A are all logic 1, the data output signal will be a logic 0 for output A and a logic 1 for output B; when a logic 0 is applied to pin 1 or 2 of U10A, indicating an out-of-phase condition, the data output signal will be logic 1 for output A and logic 0 for output B.



Radio Set Control, Using A2 642-3591-001, -002,
Functional Block Diagram
Figure 5



Modulo-Two Transmit Card A2, Timing Signals
Figure 6


2400 HZ
WT 1
WT 2
WT 4
WT 8
WT 16
WT 32
WT 64

The tune-start signal in bit-31 position is normally transmitted as logic 0. When a frequency change is initiated, the tune-start signal is transmitted as logic 1 for four to eight successive control words to indicate that a frequency change has occurred. Turning any frequency switch supplies a momentary ground to the set terminals of U3A and U3B. This sets the false output of U3B to logic 0, which is applied to pin 7 of U9. Multiplexer U9 will insert this signal into the bit-31 position in the control word. Data gate U11 inverts the data and causes a logic 1 to be transmitted in bit-31 position as long as pin 7 of U9 is at logic 0. When the ground is removed from pins 14 and 8 of U3A and U3B, two negative-going transitions of the WT64 timing signal supplied to U3A clock input (TP1) must occur before the output at pin 11 of U3B changes back to its normal state of logic 1, which causes bit 31 to return to logic 0. On later models, an input is provided to accept an external tune initiate pulse. The mode switch also has been changed to provide a tune initiate pulse during the transition from OFF to USB.

5.3.3.3 A2 642-3591-001, -002

The internal timing signals required by A2 642-3591-001, -002 are derived from the 4800-Hz oscillator (U1D and U1B). The output of the oscillator is applied to the clock circuit (U2, U9B, and U4A). The clock circuit generates a 2400-Hz clock pulse (U2-12), which is applied to U9B. At U9B, the inverting output is used to clock shift registers U5 through U8, and is combined with the control word data input at U1C. The output of U4A-1 is a logic 0 until the U2-3 output sets U4A-1 output to logic 1. The logic 0 at U4A-1 is used to load data at the parallel inputs of shift registers U5 through U8 into these registers. Once loaded, the parallel data is serially shifted out U8 pin 3, starting with the key line bit and ending with the word sync bit. Serial output (U8-3) is applied to U1C where it is combined with the 2400-Hz clock signal. This data signal is applied to line driver U9A where its output is applied to pins 38 and 40 of P1. At the end of a data word, the U2-3 output will be a logic 1; this is used to reset U2. The U4A-2 output (logic 0) is applied to U3. The U3 pin 12 output is used to supply the word sync bit to U5. The tune-start output (U4B-13) bit is normally transmitted as a logic 0. When a frequency change is initiated, the tune-start output (U4B-13) will be reset to a logic 1 by a tune initiate at U1A. This same tune-initiate signal also resets U3 to start its count at 0. The U4B output will remain at logic 1 until U4B is set by a logic 1 output of U3 pin 6 (approximately 16 control words later). This changes the tune-start signal (U4B-13) to a logic 0.

Cards A2 642-3591-001, -002 are the same, except for input power requirements. Card A2 642-3591-001 requires a +5-V dc input (W1, W2, and W3 strapped) at P1-41 and 42. Card A2 642-3591-002 requires a +15-V dc input (W4 and W5 strapped) at P1-36.

5.3.4 +15-V DC to +5-V DC Converter A1 (-0XX and -1XX Series Control Only)

The +15-V DC to +5-V DC converter A1 receives a continuous +15 V dc from the receiver-exciter, converts it to +5 V dc, and applies it to pins 41 and 42 of P1 on modulo-two transmit card A2 (793-9264-001 or 642-3591-001 only). The +15-V DC to +5-V DC converter A1 is not used on modulo-two transmit card A2 642-3591-002 as this A2 card requires +15 V dc, which is applied directly to P1-36 on the card.

5.3.5 Power On Tune Initiate Circuit (792-6122-X05, -X07)

On the 792-6122-X05 and 792-6122-X07 versions of the 514A-4, a transistor circuit was added to provide a tune initiate pulse as soon as power is applied to the unit. Refer to figures 8 through 11 in the diagrams section. As power is applied, transistor Q1 is forward biased and provides a logic 0 signal on the tune initiate line. Once capacitor C1 is charged, the base of Q1 is lowered almost to ground potential, cutting off the transistor; in this condition, the collector/emitter impedance is essentially an open circuit. Refer to table 1 in the diagrams section of this manual for effectivities information on these changes.

6. DIFFERENCE DATA

The 514A-4 Radio Set Control unit is available in a variety of configurations to suit the individual requirements of the customer. The differences between units are listed in table 2. The 514A-3 uses a different type of connector than the 514A-4 for main input/output connector J-1; connector wiring is also changed.

Table 2. 514A-3/4 Difference Data.

COLLINS PART NUMBER	PANEL COLOR	KNOB COLOR	PANEL LIGHTS		SECURE VOICE MODES	CW MODE
			COLOR	VOLTS		
514A-3 792-6121-001 (1) -101 (2) -201 (3)	Black	Black	White	28	Yes	Yes
514A-4 792-6122-001 (1) -101 (2) -201 (3)	Black	Black	White	28	Yes	Yes
792-6122-002 (1) -102 (2) -202 (3)	Black	Black	White	5	Yes	Yes
792-6122-003 (1) -103 (2) -203 (3)	Black	Black	White	5	No	No
792-6122-004 (1) -104 (2) -204 (3)	Collins 190 Gray (No 36231)	Black	Blue-white	5	No	No
792-6122-005 (1) -105 (2) -205 (3)	Boeing 703 Gray	Boeing 703 Gray	Blue-white	5	Yes	Yes
792-6122-006 (1) -106 (2) -206 (3)	Not Built					
792-6122-007 (1) -107 (2) -207 (3)	Boeing 703 Gray	Boeing 703 Gray	Blue-gray	5	No	No
792-6122-008 (1) -108 (2) -208 (3)	Not Built					
792-6122-009 (1) -109 (2) -209 (3)	Black	Black	Red	28	Yes	Yes
792-6122-010 (1) -110 (2) -210 (3)	Collins 190 Gray (No 36231)	Collins 190 Gray (No 36231)	White	28	Yes	Yes
792-6122-011 (1) -111 (2) -211 (3)	Black	Black	*White	5	Yes	Yes
792-6122-012 (1) -112 (2) -212 (3)	Black	Black	Blue-white	5	Yes	Yes

Table 2. 514A-3/4 Difference Data (Cont).

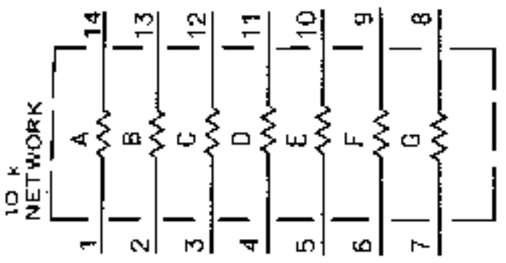
COLLINS PART NUMBER	PANEL COLOR	KNOB COLOR	PANEL LIGHTS		SECURE VOICE MODES	CW MODE
			COLOR	VOLTS		
792-6122-013 (1) -113 (2) -213 (3)	Collins 283 Gray (No 36118)	Black	Blue-white	5	No	No
792-6122-014 (1) -114 (2) -214 (3)	Collins 283 Gray (No 36118)	Collins 283 Gray (No 36118)	White	28	No	No

*Lighting per Beech spec BS22553A.

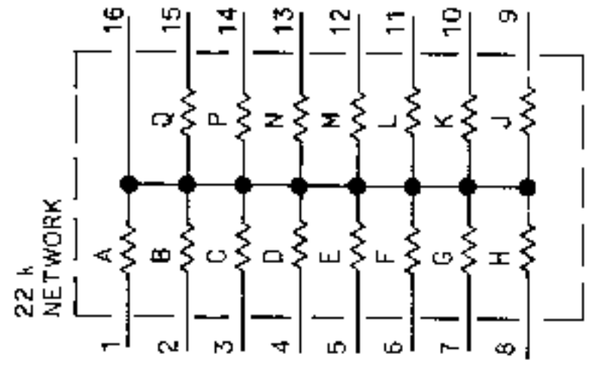
(1) This status (-0XX) uses modulo-two transmit card A2 793-9264-001 and requires dc-to-dc converter A1.
(2) This status (-1XX) uses modulo-two transmit card A2 642-3591-001 and requires dc-to-dc converter A1.
(3) This status (-2XX) uses modulo-two transmit card A2 642-3591-002 and does not required dc-to-dc converter A1.

DAMAGE.

10 k NETWORK



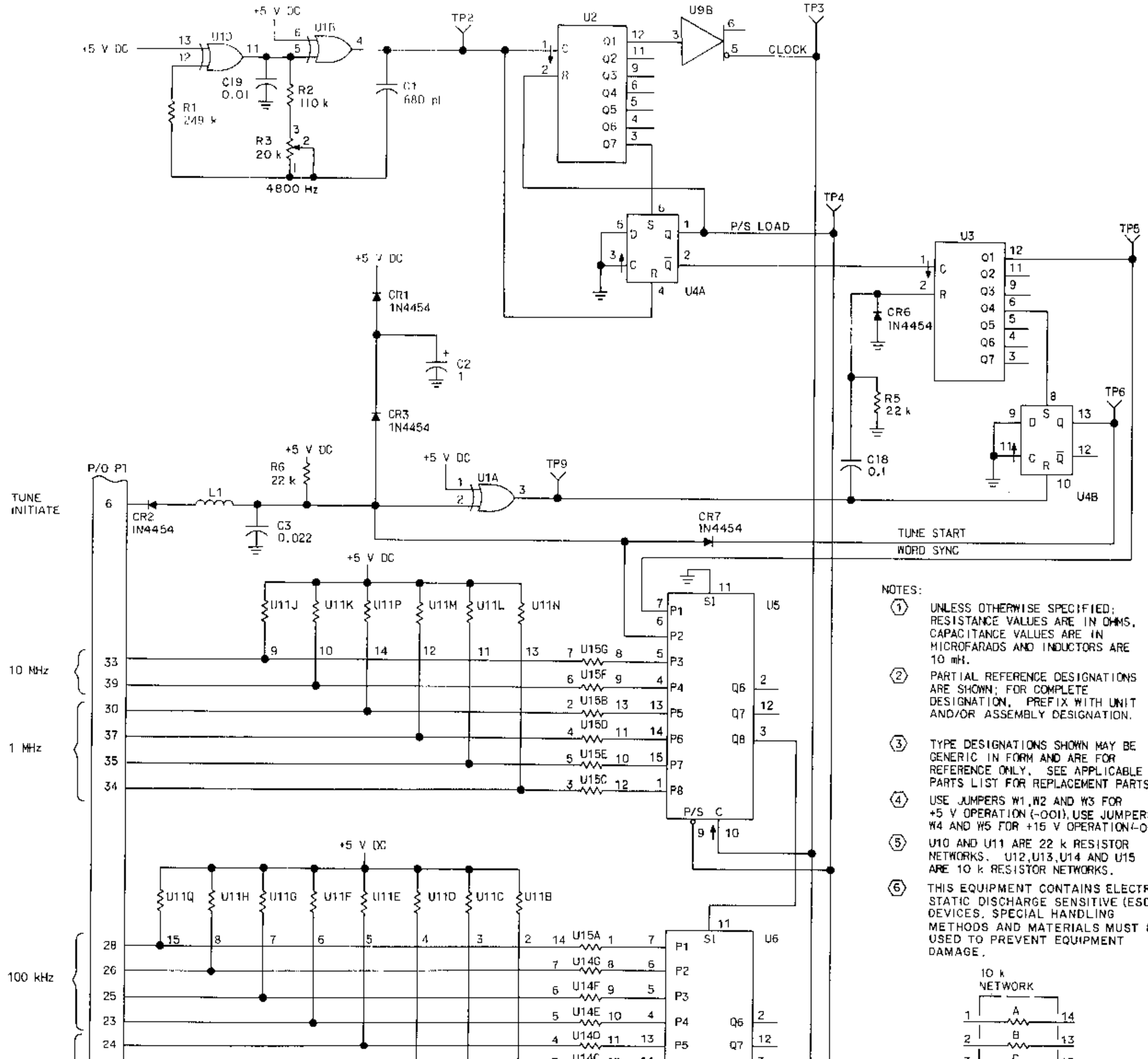
22 k NETWORK



MICROCIRCUIT INFORMATION

U NO	TYPE NO	PWR (V DC) +5	PWR (V DC) GND
U1	4070	14	7
U2	4024	14	7
U3	4024	14	7
U4	4013	14	7
U5	4021	16	8
U6	4021	16	8
U7	4021	16	8
U8	4021	16	8
U9	9638	1	4
U10		16	
U11		16	
U12			
U13			
U14			
U15			

Modulo-Two Transmit Card A2 (642-3591-001, -002).
Schematic Diagram
Figure 14



NOTES:

1. UNLESS OTHERWISE SPECIFIED; RESISTANCE VALUES ARE IN OHMS, CAPACITANCE VALUES ARE IN MICROFARADS AND INDUCTORS ARE 10 mH.
2. PARTIAL REFERENCE DESIGNATIONS ARE SHOWN; FOR COMPLETE DESIGNATION, PREFIX WITH UNIT AND/OR ASSEMBLY DESIGNATION.
3. TYPE DESIGNATIONS SHOWN MAY BE GENERIC IN FORM AND ARE FOR REFERENCE ONLY. SEE APPLICABLE PARTS LIST FOR REPLACEMENT PARTS.
4. USE JUMPERS W1, W2 AND W3 FOR +5 V OPERATION (-001). USE JUMPERS W4 AND W5 FOR +15 V OPERATION (-002).
5. U10 AND U11 ARE 22 k RESISTOR NETWORKS. U12, U13, U14 AND U15 ARE 10 k RESISTOR NETWORKS.
6. THIS EQUIPMENT CONTAINS ELECTROSTATIC DISCHARGE SENSITIVE (ESDS) DEVICES. SPECIAL HANDLING METHODS AND MATERIALS MUST BE USED TO PREVENT EQUIPMENT DAMAGE.

10 k NETWORK